ABSTRACT OF THE DISCLOSURE

A digital phase-locked loop compiler includes a pre-divider, a phase digital converter, a digital-to-analog voltage converter, a voltage-control oscillator, a high-frequency oscillator, a post-divider, an out-divider, and a built-in self-tester. The digital phase-locked loop compiler operates in a digital mode and utilizes a preset phase adjusting value to reduce phase-locking time. Moreover, the absence of a low-pass filter in the digital phase-locked loop compiler and the small size of the built-in self-tester greatly reduce the overall area of the digital phase-locked loop compiler.